Ultra-Low DC Power Consumptions in Monolithic *L*-Band Components

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Abstract—**A set of monolithic *L*-band components operating at milliwatt and sub-milliwatt dc power consumptions have been designed and fabricated . A maximum gain/power quotient of 19.1 dB/mW was recorded for a monolithic amplifier at a frequency of 1.25 GHz with a cascade of 2 MMIC amplifiers yielding a total gain of 15.3 dB on a total power consumption of just 800 μW. This is believed to be the highest gain/power quotient ever reported for a monolithic circuit at *L*-band. A four pole voltage controlled filter with low power amplifier gain stages showed a loss of 1.6 dB with 15% 3dB bandwidth on a power consumption of 6.75 mW at 1.575 GHz. A subsystem containing the chips was assembled and tested. The ultra-low power consumptions were obtained with a standard foundry process using an enhancement mode MESFET with a variety of design techniques. Yields obtained on two 4″ GaAs wafers were 96–100%.**

I. Introduction

MINIMIZATION of dc power consumption is critical for prolonged battery life in portable RF applications. Presently, commercially available MMIC amplifier chips runs at power consumptions which are an order of magnitude or more higher than what is desired for many battery operated systems. Also, many of these chips are wastefully broadband which can increase the demands on front end desensitization and image reject filters. Interest in this area has been steadily increasing [1], [2], [5] because of an expanding commercial need in personal communications products such as pagers, wireless modems, and wireless local area networks, as well as defense related applications in portable communications. Portable Global Positioning System receivers and RF tags are of interest in both the defense and commercial sectors.

II. Design

Both device/component and circuit design optimization are important in obtaining minimum dc power consumption in MMICs. All of the design methodologies in this section are oriented toward reactive (L-C) matching networks rather than lossy (R-C) matching networks due to the improved gain and noise figure performance of this type of circuit. Specific amplifier designs are not discussed in favor of a general design methodology which applies to all of the amplifiers in this study. A voltage controlled filter which incorporated alternating bandpass and low power gain stages is discussed in the last section.

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A. Device/Component Optimization

A 1 μM gate length MESFET process was chosen for this work because of its versatility and high reproducibility at the frequencies of interest. Since device transconductance is inversely proportional to device channel depth in the MESFET, shallower channel devices will yield improved performance at low power consumptions. For this reason, the gain potential of an enhancement-mode FET is superior to a depletion-mode FET at low biases given similar doping profiles. This type of device has been chosen for the circuits fabricated in this work. Other authors have previously incorporated E-mode MESFETs to achieve low dc power consumptions with excellent results [2], [3].

The device width must be chosen carefully in order to ensure the best circuit performance along with circuit yield. Smaller width devices theoretically appear to offer higher gain for the same power consumption because of their larger maximum stable gain at a particular power level; however, several factors degrade the performance as device width is decreased. At low power consumptions, as shown in Fig. 1, the device gain circles shrink as the power is reduced for a constant device width. Highly controlled element values are thus required to realize maximum device gain. Instabilities can easily result if the element values arre perturbed slightly from their intended values. In order to counteract this effect, the device width must be increased. Fig. 2 illustrates the effect of increasing the device width at a small constant power consumption of 1.50 mW. It can be seen that the low power matching problem is alleviated at larger device widths. Another problem with small width devices is that the higher impedance levels of the device require higher values of matching inductance which may translate into lower inductor Qs, higher noise figures, and lower gain. In contrast, a device which is too large will produce unacceptably small gain.

In order to determine the optimum device width, the effects of device width on circuit gain and yield are studied for an enhancement mode MESFET biased at 1 V and 1.5 mA. The *S*-parameter data was obtained by scaling data from a 300 μM device biased at Vds = 1.0 V and Ids = 1.0 to 3.0 mA in 0.5 mA increments. Data for 150, 180, 225, 300 and 450 μM devices at a power consump-

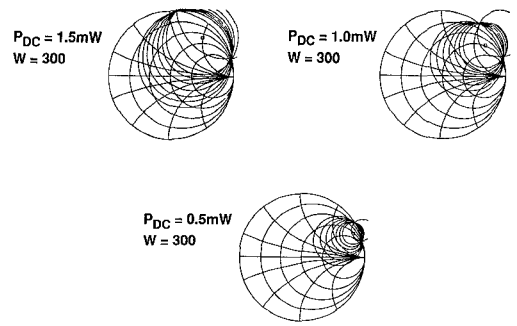


Fig. 1. Gain circles for three different device power consumptions at a constant width of 300 μM.

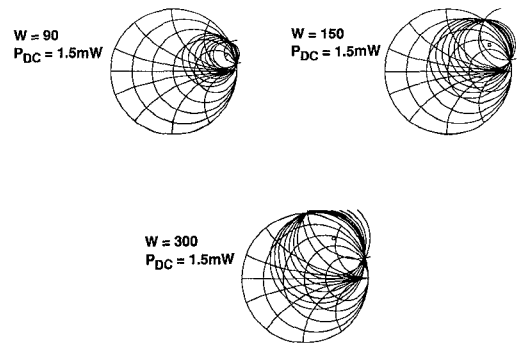


Fig. 2. Gain circles for three different device widths at a constant power consumption of 1.50 mW.

tion of 1 V and 1.5 mA was then derived from this data. Element values for a circuit with the narrowband topology discussed below were then optimized subject to the same optimization criteria for each of the device widths. Non-ideal elements were used. Monte Carlo yield analysis was then performed assuming an angular S-parameter tolerance of 10° and capacitance variation of $\pm 15\%$. A circuit was considered a failure if its gain varied by more than ± 0.5 dB or its input or output VSWR exceeded 2 : 1 at a frequency of 1 GHz. The results of these simulations are shown in Fig. 3. It can be seen that very little improvement in gain was obtained at device widths below 200 μM at the cost of a drastic reduction in circuit yield. At device widths greater than 300 μM, no improvement in yield was obtained at the cost of a large reduction in circuit gain. A device width of 300 μM was chosen since only a small improvement in gain (≈ 0.5 dB) was obtained by reducing the device width to 200 μM at the cost of approximately 1/3 of the yield.

Choice of device bias point in generally a trade-off between power consumption, size, and system dynamic range and linearity requirements. In systems that do not have stringent linearity requirements (the majority of commercial portable and satellite communications systems), the device can be operated at a point where it will yield the highest gain/power consumption. Lower gain/stage at lower power consumptions will increase the number of required stages and, therefore, the amplifier size, however, the resulting reduction in the battery size of a battery operated system may be more significant in terms

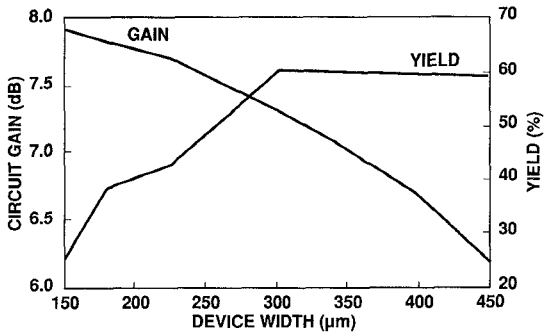


Fig. 3. Optimized circuit gain and corresponding yield vs. device width for a 1 μM enhancement mode MESFET at 1.5 mW total power consumption.

of overall size. Low power bias points may also be used in the first stages of a front end amplifier chain in a system that has higher linearity requirements so long as the overall linearity of the amplifier chain is preserved [7].

MESFETs obtain their highest gain/power efficiencies at low voltages around the "knee" (generally less than 1 V). This does not present any limitation on the use of MESFETs in systems with higher voltage supplies (typically 3 V to 5 V in battery powered systems) since device biasing can be easily achieved through voltage stacking (as demonstrated below) rather than current stacking as in conventional systems. The highest gain/power efficiencies for the 1.0 μM gate length enhancement mode MESFETs used in this work were obtained at voltages of 0.5 V and current consumptions of about 0.4 mA (total device power consumption of 200 μW).

Inductor Qs were optimized in order to realize the full potential of the minimal device gain at low power consumptions and to yield optimum noise figures. Thicker metal layers are desirable, however, when this is not an option, as with a fixed foundry process, wider line widths with narrow spacings yield higher Qs at the expense of circuit area. Fig. 4 shows a comparison of two inductors having equivalent low frequency inductance but much different geometries. The inductor Q is improved by a factor of 4 over the frequency of interest on the larger inductor. This area trade-off for performance may be acceptable given the application. The measured Q's for 2 μM metal thickness lines were between 13 and 19 for the inductors designed in this work. Typical inductor widths and spacing were 20–40 μM and 5–10 μM, respectively.

B. Amplifier Design

Two topologies, shown in Fig. 5, were used to obtain the results presented in this work. The two element matching network shown in Fig. 5(a) yields narrow band results, while the 3-element matching network gives a broader frequency response. The use of a source inductor is a standard low noise technique and is effective in shifting the noise figure circles closer to the gain circles resulting in low noise circuits with excellent gain and input match.

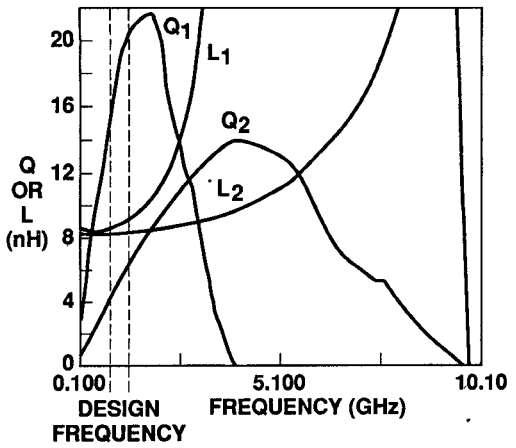


Fig. 4. Inductor values and Qs for two different size inductors; (Q1, L1) is 900 μM $\times$ 480 μM with a line width of 40 μM and spacing of 5 μM placed directly on a 25 mil GaAs substrate and (Q2, L2) is 190 μM $\times$ 190 μM with a line width and spacing of 5 μM suspended with air bridges over a 25 mil GaAs substrate.

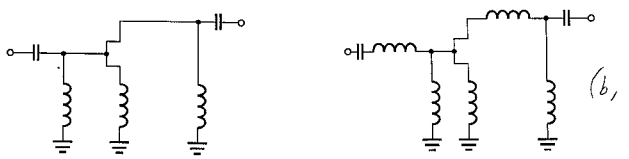


Fig. 5. (a) Narrowband and (b) broadband circuit topologies of the single-stage amplifiers fabricated in this work.

Bias networks were chosen to be efficient in terms of power consumption and at the same time allow sufficient temperature compensation and insensitivity to supply voltage variations. Active bias networks, although efficient in terms of area since they can reduce the number of required bypass capcitors, are not generally efficient in terms of power consumption. Simple resistive bias networks utilizing a source resistor were incorporated into the design in the self-biased circuits fabricated in this work. This type of network generally provides sufficient temperature compensation without the need for any additional circuitry. On board variable resistances supported operation on a variety of voltage supplies and at currents correlating to the noise figure and dynamic range requirements.

C. Voltage Controlled Filter Design

The block diagram and circuit diagram of a voltage controlled filter intended for receiver frequency hopping is shown in Fig. 6. Two single stage low power amplifiers having the topology shown in Fig. 5(a) were interspersed with two 2-pole filters. Each filter stage is a two resonator bandpass with Schottky diodes used as the voltage tuned capcacitive elements. A minimum bandwidth of 15% was determined to be a reasonable goal given the realizable Q's of the monolithic inductors and Schottky diode capacitance. The resonator inductance and capacitance values were 2.2 nH and a tunable 2.0–4.5 pF respectively. A depletion FET implant was used to form the diodes. A

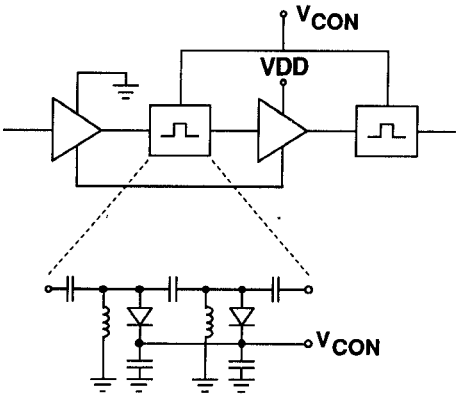


Fig. 6. (a) Block diagram of the 4-pole voltage controlled filter developed in this work and (b) circuit topology of one of the 2-pole filter blocks.

total diode area of 1200 μm $\times$ 1 μm was required to form the necessary capacitance values. Serial biasing was used for the two amplifiers stages to conserve on power consumption.

III. Results

A. Amplifier Results

Amplifiers were designed for applications in the frequency range between 900 and 1575 MHz. The lumped element designs were fabricated on 25 mil 4″ GaAs wafers without backmetallization. The results are summarized in Table I and plotted in Fig. 7 where they are compared with previously published data. The vertical scale uses a criterion which has been defined for comparison purposes as the circuit gain divided by its power consumption in mW. Input and output VSWRs of all of the amplifiers shown were better than 3 : 1 at the frequencies listed. Yields on the circuits were generally 100% with gain variations approximately $\pm$0.3 dB/stage across two four inch GaAs wafers. A more complete set of statistical variations was given in [8].

The highest gain/power quotient was obtained on a two stage amplifier operating at 1.25 GHz on a total power consumption of 400 μW. Each of the two transistors in this amplifier were biased at 0.5 V with a current consumption of 400 μA. The gain and return loss of this amplifier are shown in Fig. 8(a). A self-biased version of this amplifier operated on a single 1.5 V supply at a current consumption of 0.5 mA with a gain of about 10 dB. Both versions of the amplifier were unconditionally stable at all frequencies. The non-self-biased version was designed to be easily cascaded using voltage stacking, i.e., the MESFET source was dc floated. In order to demonstrate the stacking feature, a two chip cascade was assembled, the results of which are shown in Fig. 8(b). In this circuit four stages are biased serially from a single 2 V supply to obtain a gain of better than 15 dB on a current consumption of only 400 μA.

The lowest noise figure of 1.6 dB was obtained on a single stage amplifier which operated at 1 GHz on a power consumption of just 5 mW. Input and output VSWRs were

TABLE I
TABULATED RESULTS FOR THE AMPLIFIERS DEVELOPED IN THIS STUDY

Circuit Description	Freq (GHz)	Bias Condition	P_{DC} (mW)	G (dB)	NF (dB)	Size (in^2)
1 GHz LNA	1.0	2.5 V @ 2 mA	5.0	10.3	1.6	0.52 × .112
	1.0	1 V @ 0.5 mA	0.5	6.0	2.5	
1 GHz Self-Biased Narrow-Band 2-Stage LNA	1.0	5 V @ 2 mA	10.0	19.6	2.2	.112 × .112
	0.9	2.5 V @ 0.5 mA	1.25	9.2	4.8	
Self-Biased GPS LNA	1.575	5 V @ 2 mA	10.0	8.5	1.7	.052 × .112
	1.575	2.5 V @ 1 mA	2.5	6.0	2.0	
2-Stage Amplifier	1.25	1 V @ .4 mA	0.41	7.2	6.0	.080 × .112
2-Stage Self-Biased Amplifier	1.25	1.5 V @ 0.5 mA	0.75	10.0		.080 × .112
Self-Biased GPS 2-Stage LNA	1.575	5 V @ 2 mA	10.0	17.4	2.2	.080 × .112
	1.575	2.5 V @ 0.5 mA	1.25	9.0	3.8	
Narrow-Band GPS LNA	1.575	2.5 V @ 2 mA	5.0	7.5	2.2	.052 × .052

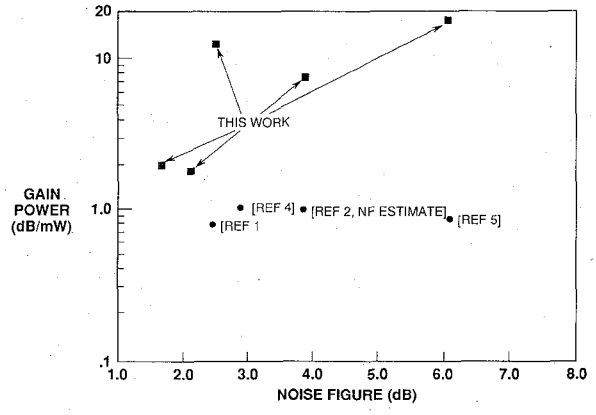
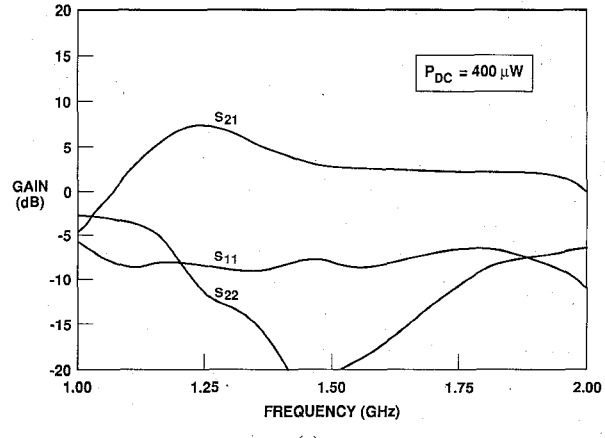
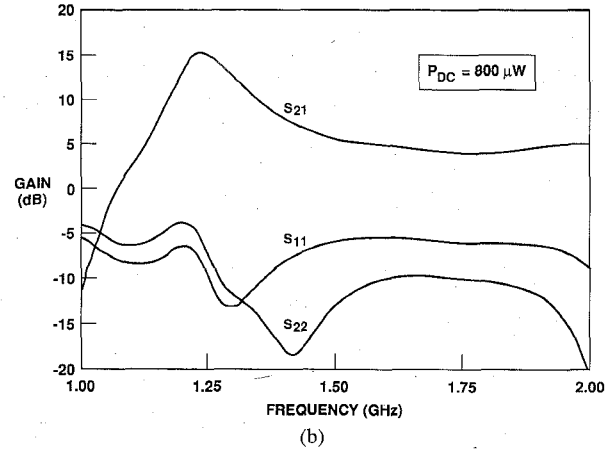


Fig. 7. Comparison of the results of the LNAs designed and fabricated in this work with previously published results.



(a)



(b)

Fig. 8. (a) Gain and return loss of a two-stage low power MMIC amplifier biased at 1 V and 0.4 mA and (b) results for a two chip cascade of the circuit in (a) with 4 stage voltage stacking resulting in a total bias of 2 V at 0.4 mA.

better than 2:1. This amplifier used the broadband topology shown in Fig. 5(b) and had a usable bandwidth between 0.7 and 1.3 GHz. The transistor used in this circuit was a 450 μM width enhancement mode MESFET. This same amplifier operated at 500 μW with a noise figure of 2.5 dB and a gain of 6 dB. In order to demonstrate the feasibility of a low power transmitter for short range applications, this amplifier circuit was also characterized for large signal operation. Figure 9 shows measured power added efficiency and power output for the circuit. The nominal small signal bias condition for the amplifier was 2.5 V @ 2 mA. Gain is shown in Fig. 10. A maximum power added efficiency at 1 dB compression of 34% was obtained when the circuit was operated in class AB mode. Although the circuit was not specifically designed for large signal operation, its results demonstrate that reasonable efficiencies and gain can be achieved at very low power bias conditions.

Gain and noise figure for the self-biased two stage amplifier targeted for GPS applications are shown in Fig. 11. This amplifier had the topology illustrated in Fig. 5(b). The FETs were biased in series and an on-board variable bias network was available to adjust the amplifier to operate on different supply voltages and currents. The data for two bias conditions are illustrated. Input and output VSWRs were better than 3:1. The measured 1 dB compression point at 1.575 GHz was −2 dBm at 10 mW power consumption and −16 dBm at 1.25 mW power consumption.

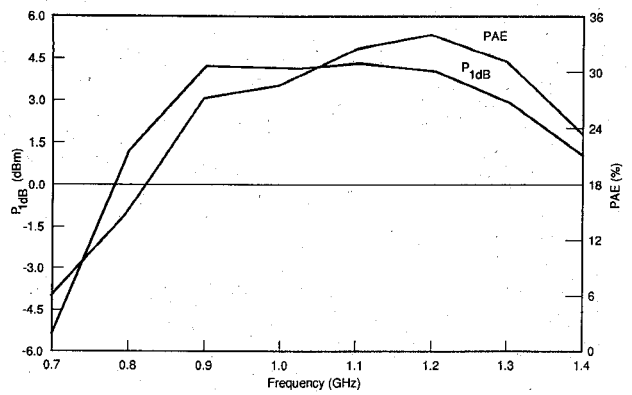


Fig. 9. Power added efficiency and output power at 1 dB gain compression for the low power broadband LNA.

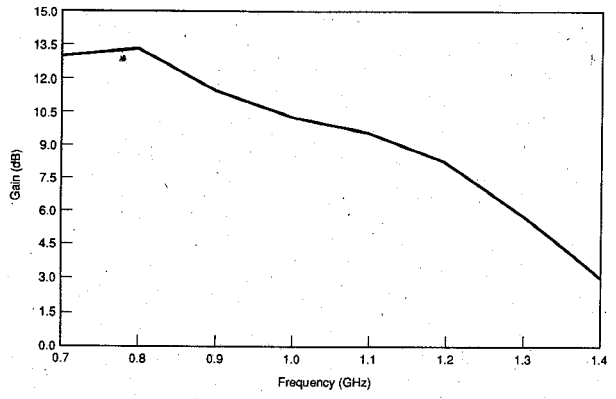


Fig. 10. Gain at 1 dB compression for the low power broadband LNA.

B. Filter Results

The 4-pole voltage controlled filter was mounted in a test fixture and characterized. A single supply voltage of 5 V was used to bias the amplifier stages. The total current from this supply was 1.35 mA for a total filter power consumption of 6.75 mW.

Frequency response and return loss as a function of the tuning voltage are shown in Fig. 12(a) and (b), respectively. The center frequency was tunable from 1.575 to 1.9 GHz with a tuning voltage ranging from −0.5 to 1.0 V. The bandwidth increased from 15% to 20% and the loss of the individual filter stages decreased as the center frequency increased. The overall filter response showed an initial decrease in loss as the center frequency was increased followed by an increase in loss at higher center frequencies. The latter increase in loss is due to the dominance of the amplifier response which exhibits a gain rolloff at frequencies beyond 1.5 GHz. The total loss varied from 0 to 3 dB over the frequency range.

The measured Q's for the 2.2 nH inductors used in the filter stages was 12 at 1.7 GHz. The low Q's resulted in maximum filter loss of about 7 dB for each of the 2-pole filter blocks. This loss was compensated by the amplifier stages. The diode capacitance varied from 2.0 pF to 4.8 pF with a Q of 54.2 to 16.8 as the voltage varied from −1.0 to 0.5 V.

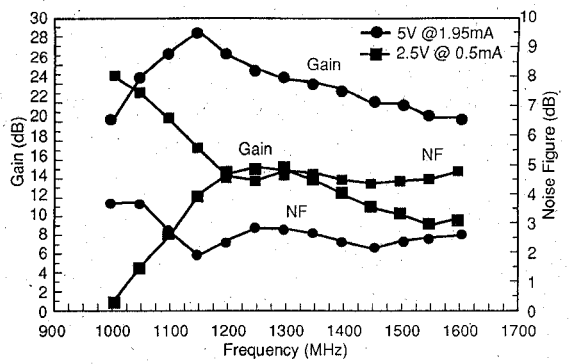
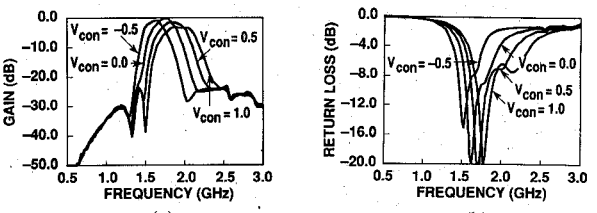


Fig. 11. Gain and noise figure for the 2-stage GPS amplifier.



(a) (b)

Fig. 12. (a) Frequency response and (b) return loss for the 4-pole voltage controlled filter tuned to center frequencies from 1.575 GHz to 1.9 GHz.

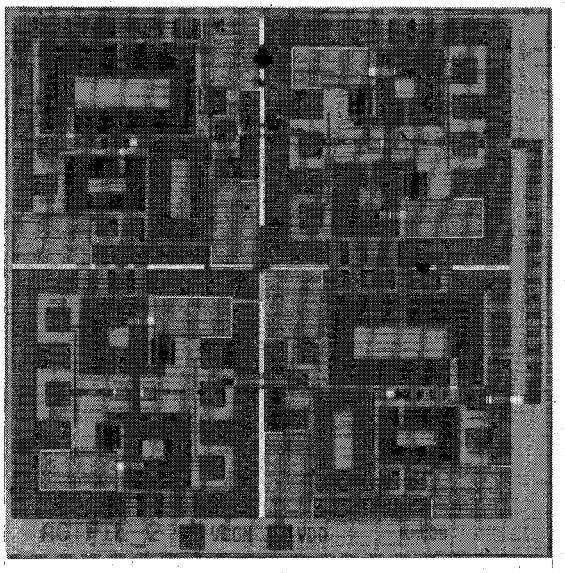


Fig. 13. Photograph of the 4-pole voltage controlled low power MMIC filter.

The filter was unidirectional due to the amplifier stages and showed a reverse transmission loss of greater than 25 dB. The size of each of the amplifier stages and each of the 2-pole filters in the layout is 1.3 mm × 1.3 mm. The fully integrated chip measured 2.8 mm × 2.8 mm and is shown in Fig. 13.

C. Module Results

A subsystem module was assembled using amplifier chips developed in this work. Two of the two-stage narrowband LNAs whose results were described in [8] were

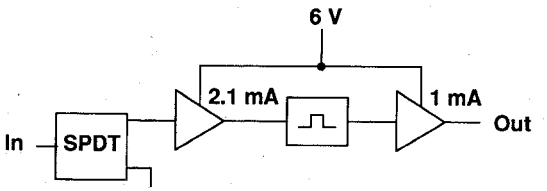


Fig. 14. Block diagram of the subsystem module formed with low power MMIC amplifiers.

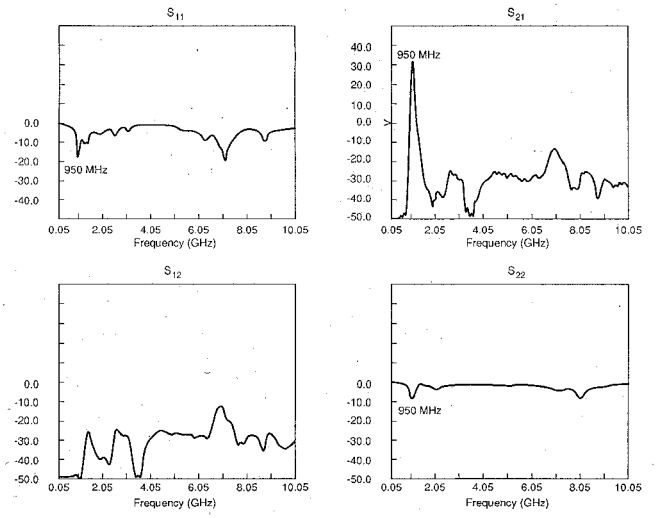


Fig. 15. Gain and return loss for the MMIC module.

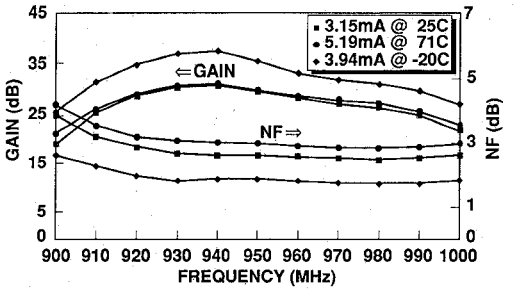


Fig. 16. Gain and noise figure for the MMIC module as a function of temperature.

combined with an interstage bandpass filter and commercial MMIC SPDT switch to form a subsystem module as illustrated in the block diagram of Fig. 14. The 25 mil thick GaAs chips were mounted on a 10 mil alumina substrate which contained via holes to ground. The interstage filter was also mounted to the alumina substrate in between the two amplifier chips and consisted of discrete inductors and capacitors. The alumina substrate containing the filter and LNAs was mounted on a test fixture with SMA connectors.

The gain and return loss from 50 MHz to 10.05 GHz is shown in Fig. 15. The module operated on a single 6 V supply with a total power consumption of 18.3 mW. The maximum gain for the module was 33 dB at 940 MHz which included about 5 dB of filter loss and 0.5 dB of switch loss. The 3 dB bandwidth for the subsystem was 40 MHz. Gain and noise figure variations as a function of temperature are shown in Fig. 16. Due to the temperature compensation of the mixed thin film and implanted resistor bias networks of the monolithic amplifiers, very little degradation in performance was observed as the temperature was increased. The size of the integrated module was .375″ × .450″.

IV. Conclusion

A set of monolithic amplifiers operating on dc power consumptions of a few milliwatts down to less than a milliwatt have been demonstrated. In addition, a monolithic low power filter was demonstrated. The components were fabricated using a standard production ready foundry process and have achieved yields approaching 100%. Power consumption reduction in MMIC components is critical for the reduction of the overall size and cost of portable RF equipment.

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In the fall of 1985 he held a temporary research appointment with CNRS in Orsay, France where he worked on the circuit simulation of GaAs digital circuits. In 1987 he joined Rockwell International where he was responsible for MMIC design, device modeling and characterization, and the application of optical devices to microwave systems. He has recently joined Wireless Access in Redwood City, CA where he is Director of Engineering and has the responsibility for the RF development of wireless data products for commercial applications.